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Sheet 1 of 1

| Complete if Known | |
|---|---|
| Application Number | Unknown / |
| Filing Date | October 07, 2003 |
| First Named Inventor | John K. Jennings |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | X-1339 US |

## OTHER -- NON PATENT LITERATURE DOCUMENTS

| Examiner Initials * | Cite No[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
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| | | Lee, Thomas H. et al.; "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabytes/s DRAM"; IEEE Journal of Solid-State Circuits, Vol. 29, NO. 12, December 1994; pp. 1491-1496. | |
| | | Maneatis, John G.; "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques"; IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996; pp. 1723-1732. | |
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| | | Bult, Klaas et al.; "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm$^2$; IEEE Journal of Solid-State Circuits, Vol. 32, No. 12, December 1997; pp. 1887-1895. | |
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